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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,548	09/30/2003	Saikumar Jayaraman	42P17182	7674

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EXAMINER	
NORRIS, JEREMY C	

ART UNIT	PAPER NUMBER
2841	

DATE MAILED: 03/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/676,548	JAYARAMAN ET AL.	
	Examiner	Art Unit	
	Jeremy C. Norris	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 April 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4-19-04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to because the sectional views are not properly crosshatched (see MPEP 608.02). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an

improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:
(1) if a machine or apparatus, its organization and operation;
(2) if an article, its method of making;
(3) if a chemical compound, its identity and use;
(4) if a mixture, its ingredients;
(5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract of the disclosure is objected to because of the use of the phrase "are provided". Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 10, and 17-20 are rejected under 35 U.S.C. 102(b) as being anticipated by US 6,282,094 (Lo).

Lo discloses, referring primarily to figure 1, an electronic assembly comprising; a circuit board (not shown but referred to, see col. 4, lines 20-40); a package substrate (31), having first and second sides, attached to the circuit board (see col. 4, lines 20-40); a plurality of contact formations (317) on the first side of the package substrate interconnecting the circuit board and the package substrate (see col. 4, lines 20-40); a stress relief layer (34) on the first side of the package substrate, a space being defined between the stress relief layer and the circuit board (see col. 4, lines 25-35); and a microelectronic die (32), having an integrated circuit formed therein, mounted on the second side of the package substrate **[claim 1]** , wherein each contact formation has a height and the stress relief layer has a thickness, the thickness of the stress relief layer being less than the height of the contact formations (see col. 4, lines 25-35) **[claim 2]**, wherein the stress relief layer is adjacent to a portion of the contact formations that corresponds to only a portion of the height of the contact formations (see figure 1) **[claim 3]**.

Additionally, Lo discloses, referring primarily to figure 1, an electronic assembly, comprising: a package substrate (31) having first and second sides; a microelectronic die (32) mounted to the first side of the package substrate; a plurality of contact formations (317) attached to the second side of the package substrate, each having a

height; and a stress relief layer (34) on the second side of the package substrate, the layer having a thickness less than the height of the contact formations (see col. 4, lines 25-35) and being adjacent to only a portion of the height of the contact formations (see fig 1) [**claim 10**].

Also, Lo discloses, referring primarily to figure 1, a method of constructing an electronic assembly, comprising: depositing a stress relief layer (34) on a side of a package substrate (31), the side having a plurality of contacts formations (317) thereon; and attaching the contact formations to a circuit board, a space being defined between the stress relief layer and the circuit board (see col. 4, lines 25-35) [**claim 17**], wherein a microelectronic die (32) is mounted on an opposing side of the package substrate [**claim 18**], wherein the contacts have a height and the stress relief layer has a thickness, the thickness of the stress relief layer being less than the height of the contact formations (see col. 4, lines 25-35) [**claim 19**], wherein the stress relief layer is adjacent to a portion of the contact formations that corresponds to only a portion of the height of the contact formations (see figure 1) [**claim 20**].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lo in view of US 6,160,224 (Ogashiwa).

Lo discloses the claimed invention as described above except Lo does not specifically state that the heights of the contact formations are between 0.2 and 1.5 mm [**claim 4**]. However, it is well known in the art to make BGA solder bumps in that range as evidenced by Ogashiwa (see col. 6, lines 25-35). Therefore, it would have been obvious, to one having ordinary skill in the art, at the time of invention, to form the solder ball in the invention of Lo to be between 0.2 and 1.5mm as is well known in the art and

evidenced by Ogashiwa. The motivation for doing so would have been to form a bump having sufficient height to ensure a reliable electromechanical connection while keeping the height profile as small as possible to reduce the overall size of the device

Claims 5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lo in view of Ogashiwa as applied to claim 3 above, and further in view of US 2002/0179289 (Yamashita).

Lo in view of Ogashiwa discloses the claimed invention as described above except it does not specifically teach wherein the stress relief layer is polymeric [**claim 5**]. Instead, it is generically taught that the layer is thermally conductive (see Lo, col. 4, lines 20-30). Yamashita teaches using a thermally conductive thermoplastic adhesive [**claim 6**] resin to draw heat away from a heat producing device (see abstract). Therefore, it would have been obvious, to one having ordinary skill in the art, at the time of invention, to use the thermoplastic taught by Yamashita in the invention of Lo as modified by Ogashiwa. The motivation for doing so would have been to use a highly thermal conductive material that is additionally electrically insulating which helps avoid undesired shorting

The twice-modified invention of Lo also does not specifically state that the thickness of the relief layer is between 0.15mm and 0.225mm [**claim 7**], rather it generically teaches that the thickness must be less than the selected contact formation height. It would have been obvious, to one having ordinary skill in the art, at the time of invention, to make the thickness of the relief layer in this range since the range overlaps

with the taught range of being less than the range of contact formation height. The motivation for doing so would have been to ensure proper thermal conduction while avoiding exceeding the height of the contact formation and interfering with the circuit board patterns. Additionally, the combined teachings of Lo and Ogashiwa and Yamashita teach wherein the space is an air space (see Lo, col. 4, lines 25-35) **[claim 8]**

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lo in view of Ogashiwa, in further view of Yamashita as applied to claim 8 above, and further in view of US 6,219,241 (Jones).

The thrice-modified invention of Lo discloses the claimed invention except that it does not specifically teach that the die is a microprocessor **[claim 9]**, instead generically teaching that the die is an IC. However, it is well known in the art that ICs may comprise microprocessors as evidenced by Jones (see col. 1, lines 10-25). Therefore, it would have been obvious, to one having ordinary skill in the art, at the time of invention, to use a microprocessor as the IC in the modified invention of Lo as is well known in the art and evidenced by Jones. The motivation for doing so would have been to make the device suitable to a computer environment.

Claims 11, 12 and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lo in view of Jones.

Lo discloses the claimed invention as described above with respect to claim 10 except Lo does not specifically teach that the die is a microprocessor [**claim 11**], instead generically teaching that the die is an IC. However, it is well known in the art that ICs may comprise microprocessors as evidenced by Jones (see col. 1, lines 10-25). Therefore, it would have been obvious, to one having ordinary skill in the art, at the time of invention, to use a microprocessor as the IC in the modified invention of Lo as is well known in the art and evidenced by Jones. The motivation for doing so would have been to make the device suitable to a computer environment. Additionally, the modified invention of Lo teaches that the contact formations are BGA solder balls (see col. 4, lines 25-35) [**claim 12**].

Similarly, Lo discloses, referring primarily to figure 1, an electronic assembly comprising; a circuit board (not shown but referred to, see col. 4, lines 20-40); a package substrate (31), having first and second sides, attached to the circuit board (see col. 4, lines 20-40); a plurality of contact formations (317) on the first side of the package substrate interconnecting the circuit board and the package substrate (see col. 4, lines 20-40); a stress relief layer (34) on the first side of the package substrate, a space being defined between the stress relief layer and the circuit board (see col. 4, lines 25-35); and a microelectronic die, mounted on the second side of the package substrate Lo does not specifically teach that the die is a microprocessor [**claim 14**], instead generically teaching that the die is an IC. However, it is well known in the art that ICs may comprise microprocessors as evidenced by Jones (see col. 1, lines 10-25). Therefore, it would have been obvious, to one having ordinary skill in the art, at the time

of invention, to use a microprocessor as the IC in the modified invention of Lo as is well known in the art and evidenced by Jones. The motivation for doing so would have been to make the device suitable to a computer environment.

Additionally, although Lo only generically states that the circuit board is a PCB, it is well known in the art that PCBs may comprise motherboards [**claim 15**] as evidenced by Jones (see col. 1, lines 10-25). Therefore, it would have been obvious, to one having ordinary skill in the art, at the time of invention, to use a motherboard as the PCB in the modified invention of Lo as is well known in the art and evidenced by Jones. The motivation for doing so would have been to make the device suitable to a computer environment. Moreover, the combined teachings of Lo and Jones disclose the stress relief layer adjacent to the contact formations (see Lo, fig. 1) [**claim 16**]

Claim 13 is are rejected under 35 U.S.C. 103(a) as being unpatentable over Lo in view of Jones as applied to claims 11 and 12 above, and further in view of Yamashita.

Lo in view of Jones the claimed invention as described above except it does not specifically teach wherein the stress relief layer is polymeric [**claim 13**]. Instead, it is generically taught that the layer is thermally conductive (see Lo, col. 4, lines 20-30). Yamashita teaches using a thermally conductive thermoplastic adhesive resin to draw heat away from a heat producing device (see abstract). Therefore, it would have been obvious, to one having ordinary skill in the art, at the time of invention, to use the thermoplastic taught by Yamashita in the invention of Lo as modified by Jones. The

motivation for doing so would have been to use a highly thermal conductive material that is additionally electrically insulating which helps avoid undesired shorting.

Claims 21-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lo in view of Yamashita.

Lo discloses the claimed invention as described above except it does not specifically teach wherein the stress relief layer is polymeric **[claim 21]**. Instead, it is generically taught that the layer is thermally conductive (see Lo, col. 4, lines 20-30). Yamashita teaches using a thermally conductive thermoplastic adhesive resin to draw heat away from a heat producing device (see abstract). Therefore, it would have been obvious, to one having ordinary skill in the art, at the time of invention, to use the thermoplastic taught by Yamashita in the invention of Lo. The motivation for doing so would have been to use a highly thermal conductive material that is additionally electrically insulating which helps avoid undesired shorting. Furthermore, the modified invention of Lo teaches wherein the stress relief layer is only deposited onto selected portions of the side of the package substrate (see Lo figure 1) **[claim 22]**, wherein the stress relief layer flows onto the package substrate (see Lo col. 5, lines 25-40) **[claim 23]**, wherein the stress relief layer is first deposited onto a central portion of the side of the package substrate (see figure 1) **[claim 24]**, wherein the stress relief layer is extruded onto the side of the side of the package substrate **[claim 25]**.

Claims 27-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,706,558 (Nakamura) in view of Lo.

Nakamura discloses, referring primarily to figure 6A, a method comprising: placing a plurality of semiconductor packages on a support (11) the semiconductor packages each having a package substrate (14) with a first side having a microelectronic die (17) mounted thereon and a second side with a plurality of contact formations connected thereto (23), the contact formations having a height. Nakamura does not specifically disclose suspending a stencil over the semiconductor packages, the stencil having a plurality of holes; and flowing a paste through the holes of the stencil to form a stress relief layer on the second side of the package substrate of each semiconductor package, the stress relief layer having a thickness, the thickness being less than the height of the contact formations. However, Lo teaches depositing a stress relief layer on package substrates to a height less than contact formations (see col. 4, lines 20-40). Therefore, it would have been obvious, to one having ordinary skill in the art, at the time of invention, to deposit the stress relief layer taught by Lo onto the invention of Nakamura. The motivation for doing so would have been to more effectively siphon heat away from the IC thus reducing the thermal stresses. Additionally, it would have been obvious, to one having ordinary skill in the art, at the time of invention, to use screen printing (stencils) as the method of relief layer deposition, since Nakamura teaches this is an effective process for selective deposition (see col. 5, lines 50-60) [**claim 27**]. The motivation for doing so would have been to use a simple process which can form all the relief layers simultaneously, thus reducing the required processing time.

The combined disclosures of Nakamura and Lo additionally teach, further comprising placing the semiconductor packages onto circuit boards, the contact formations interconnecting the package substrates and the circuit board, a space being defined between the circuit board and the second side of the package substrate (see Lo col. 4, lines 25-35) [**claim 28**], wherein the stress relief layer is adjacent to a portion of the contact formations that corresponds to only a portion of the height of the contact formations (see Lo figure 1) [**claim 29**], wherein the second sides of the package substrates face the stencil (see Nakamura col. 5, lines 50-60) [**claim 30**].

Allowable Subject Matter

Claim 21 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: Claim 21 states the limitation "wherein the stress relief layer is a cast film, having a plurality of holes therein and said depositing is placing the cast film on the side of the package substrate so that the contact formations extend through the holes". This limitation, in conjunction with the other claimed limitations was neither found to be disclosed in, nor suggested by the prior art.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeremy C. Norris whose telephone number is 571-272-1932. The examiner can normally be reached on Monday - Friday, 9:30 am - 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JCSN

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